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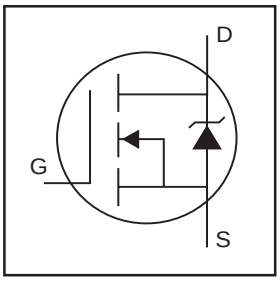
International
IOR Rectifier

PD - 91318B

IRFR/U1205

HEXFET® Power MOSFET

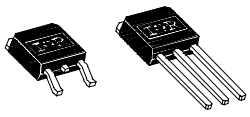
- Ultra Low On-Resistance
- Surface Mount (IRFR1205)
- Straight Lead (IRFU1205)
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

$R_{DS(on)}$ = 0.027Ω

I_D = 44A⑤



D-PAK
TO-252AA

I-PAK
TO-251AA

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	44⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	31⑤	
I_{DM}	Pulsed Drain Current ①⑦	160	
P_D @T_C = 25°C	Power Dissipation	107	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑦	210	mJ
I_{AR}	Avalanche Current①⑦	25	A
E_{AR}	Repetitive Avalanche Energy①⑦	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.055	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.027		V_{GS} = 10V, I_D = 26A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	17	—	—	S	V_{DS} = 25V, I_D = 25A⑦
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	65	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	—	—	12		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	27		V_{GS} = 10V, See Fig. 6 and 13 ④⑦
$t_{d(on)}$	Turn-On Delay Time	—	7.3	—	ns	V_{DD} = 28V
t_r	Rise Time	—	69	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		R_G = 12Ω
t_f	Fall Time		60			R_D = 1.1Ω, See Fig. 10 ④⑦
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑥
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	410	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz, See Fig. 5⑦

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	44⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑦	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	65	98	ns	T_J = 25°C, I_F =25A
Q_{rr}	Reverse RecoveryCharge	—	160	240	nC	di/dt = 100A/µs ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 470µH R_G = 25Ω, I_{AS} = 25A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 320A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A

⑥ This is applied for I-PAK, Ls of D-PAK is measured between lead and center of die contact

⑦ Uses IRFZ44N data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

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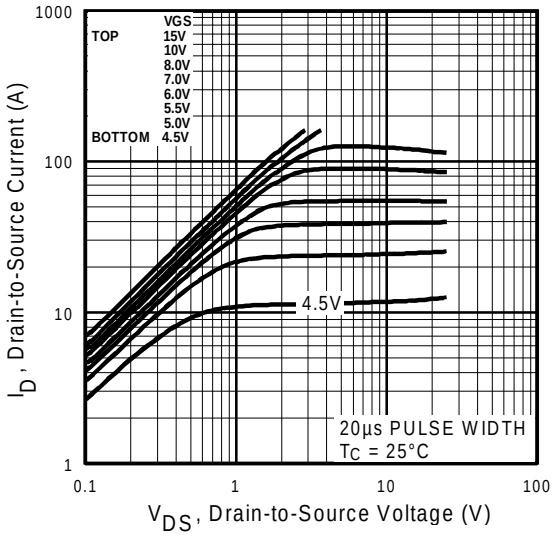


Fig 1. Typical Output Characteristics

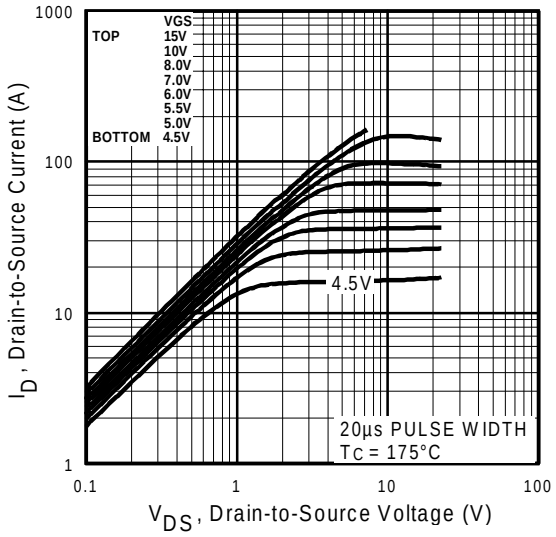


Fig 2. Typical Output Characteristics

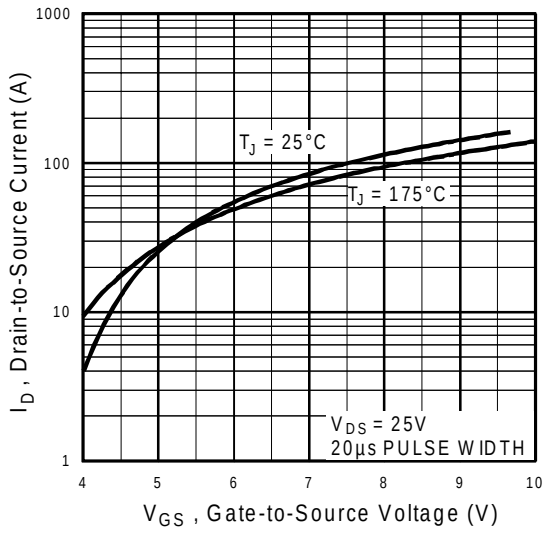


Fig 3. Typical Transfer Characteristics

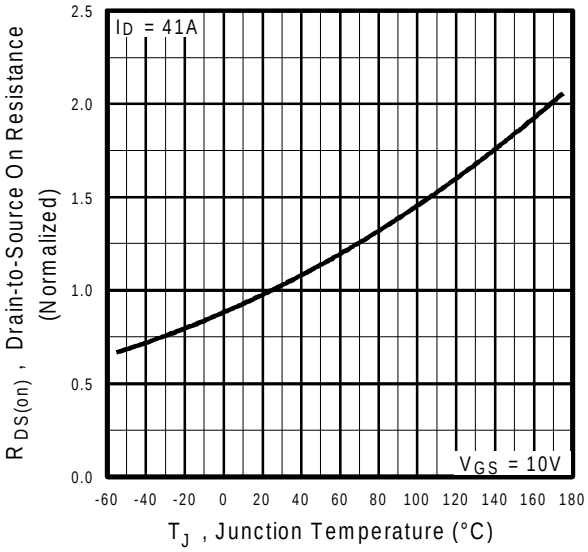


Fig 4. Normalized On-Resistance
Vs. Temperature

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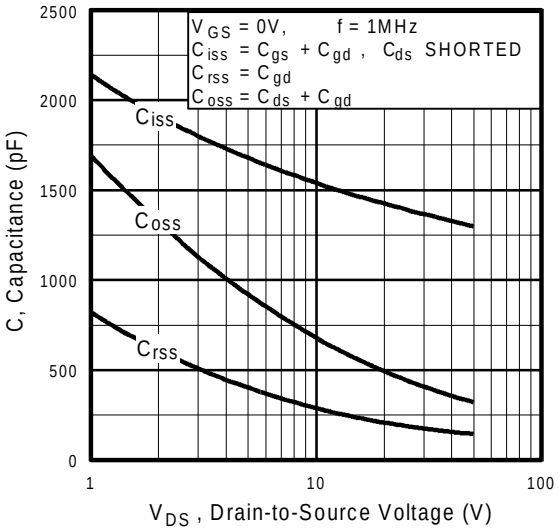


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

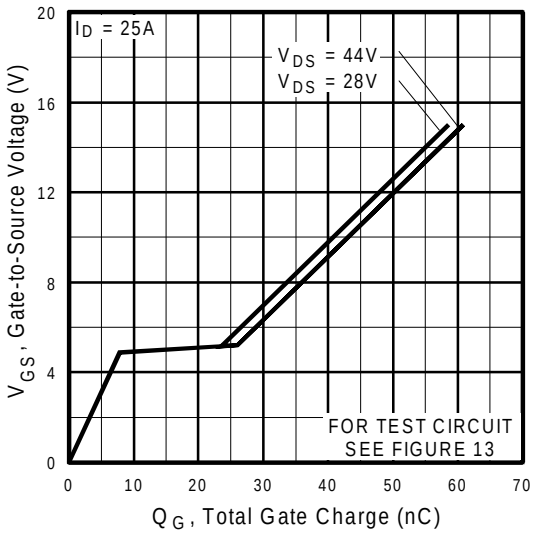


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

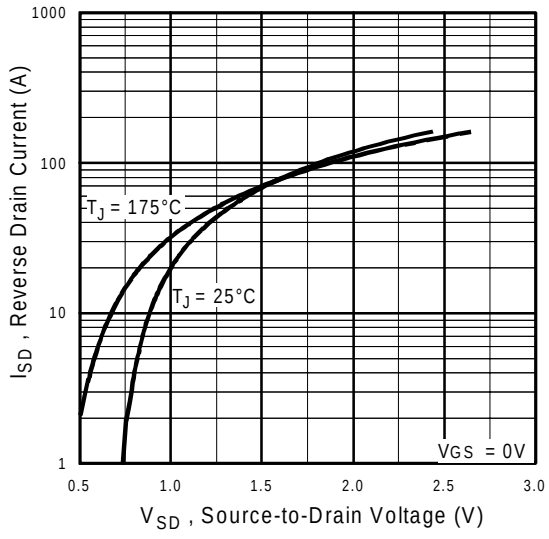


Fig 7. Typical Source-Drain Diode Forward Voltage

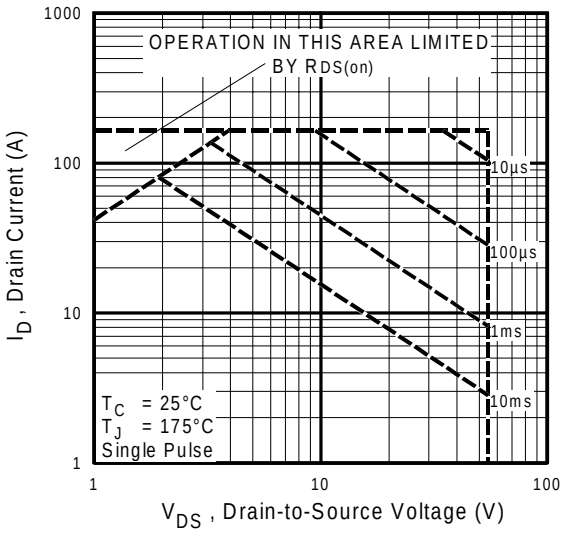


Fig 8. Maximum Safe Operating Area

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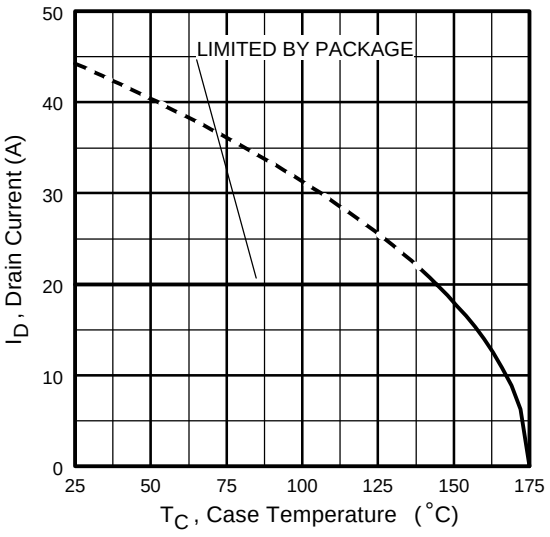


Fig 9. Maximum Drain Current Vs. Case Temperature

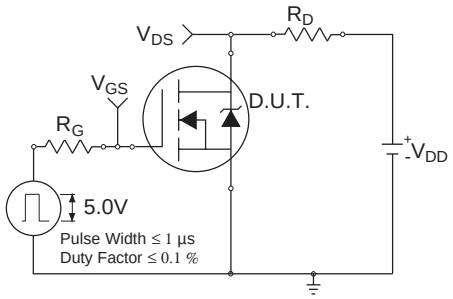


Fig 10a. Switching Time Test Circuit

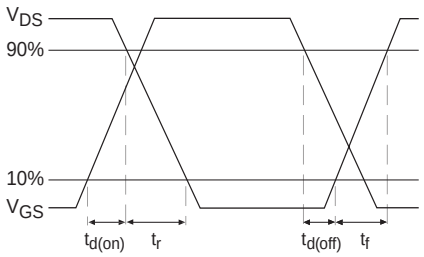


Fig 10b. Switching Time Waveforms

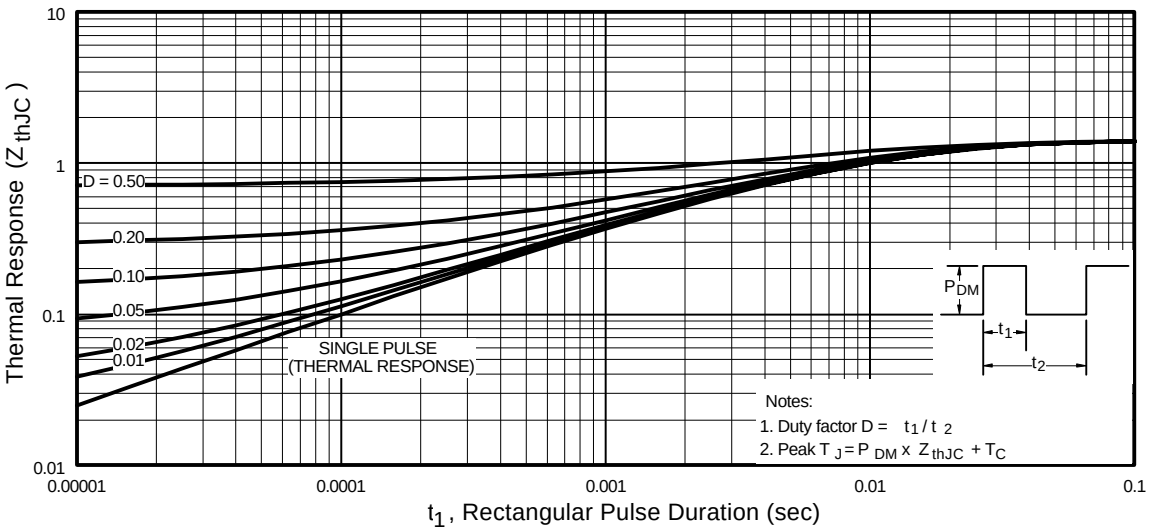


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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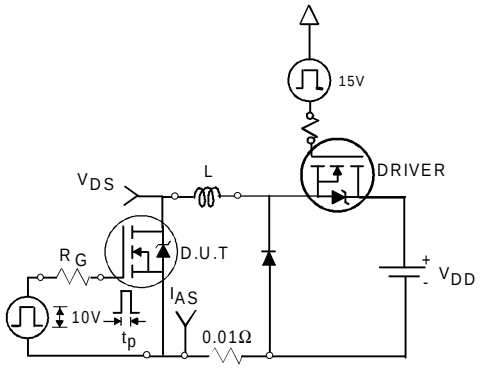


Fig 12a. Unclamped Inductive Test Circuit

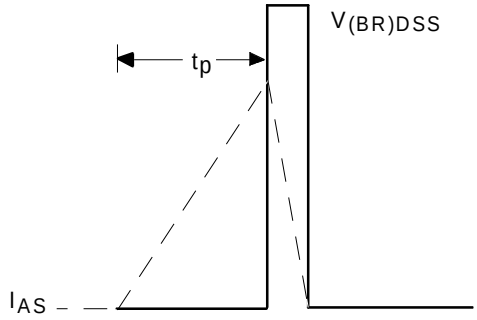


Fig 12b. Unclamped Inductive Waveforms

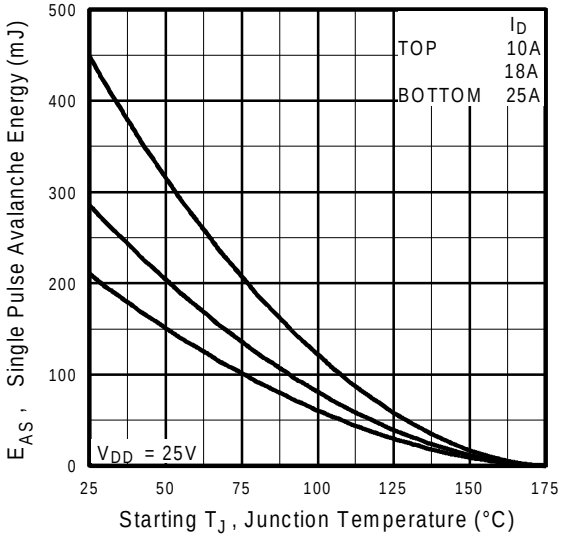


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

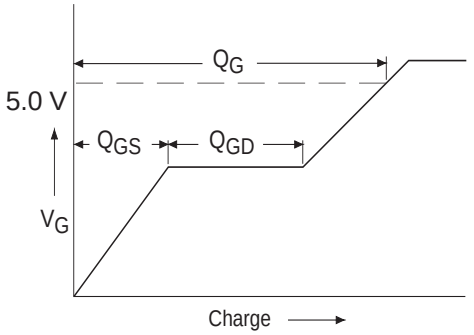


Fig 13a. Basic Gate Charge Waveform

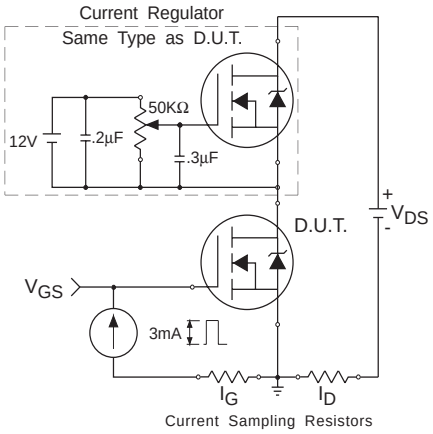
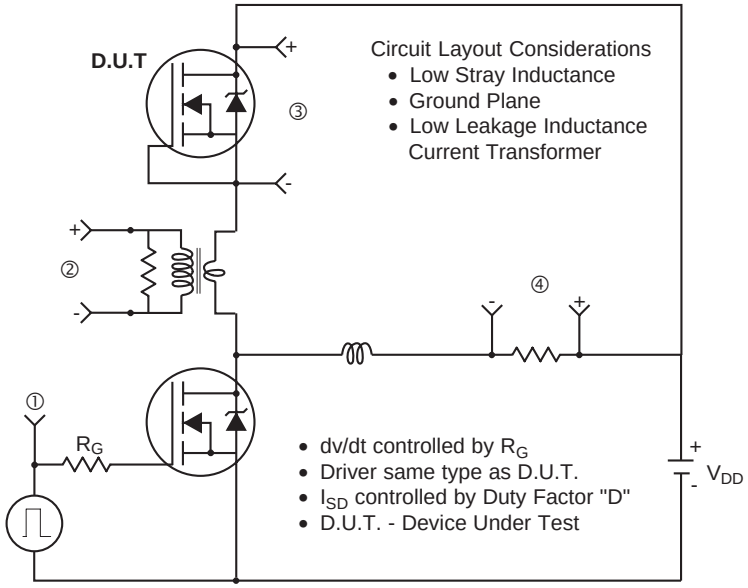
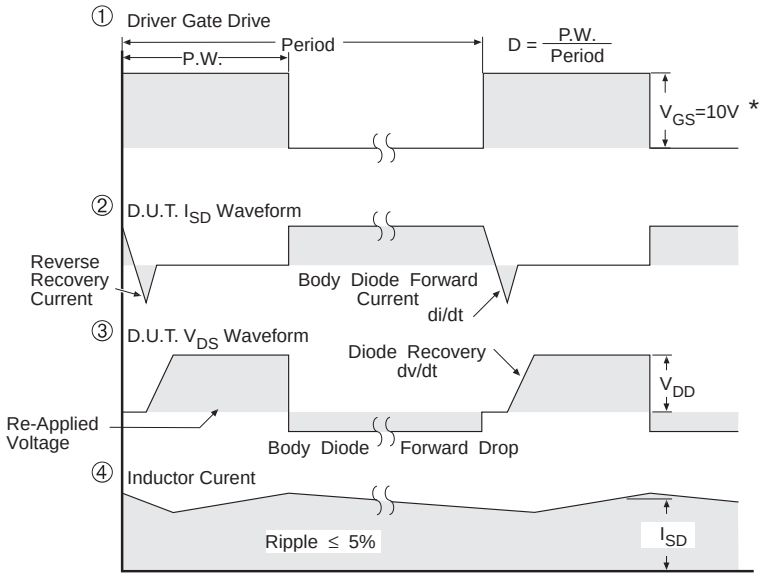


Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit





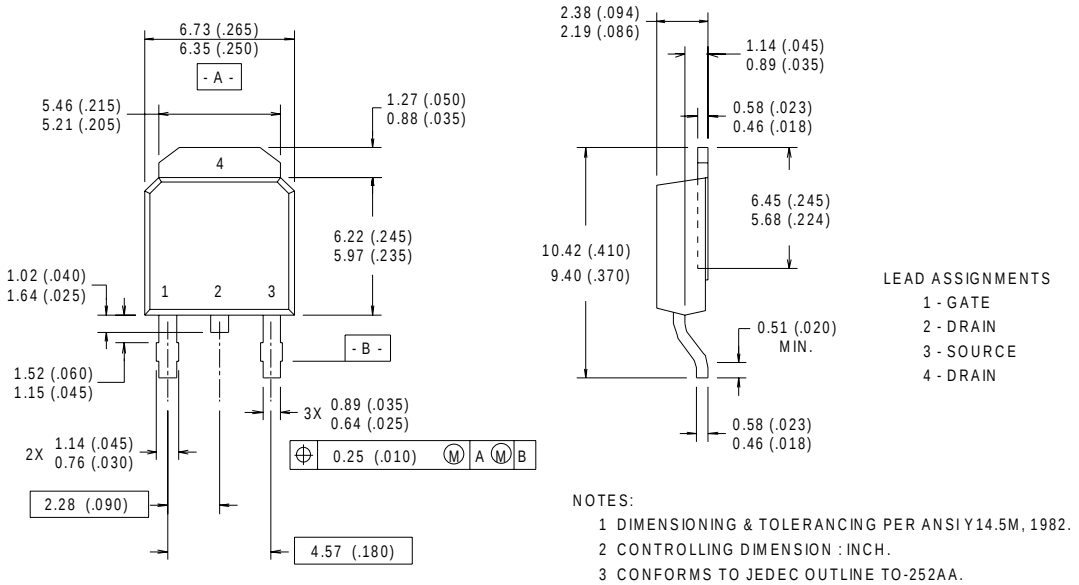
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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Package Outline

TO-252AA Outline
Dimensions are shown in millimeters (inches)

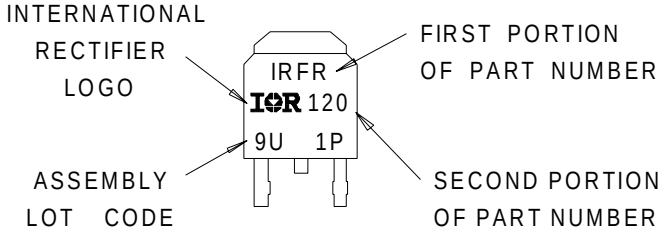


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-252AA (D-PARK)

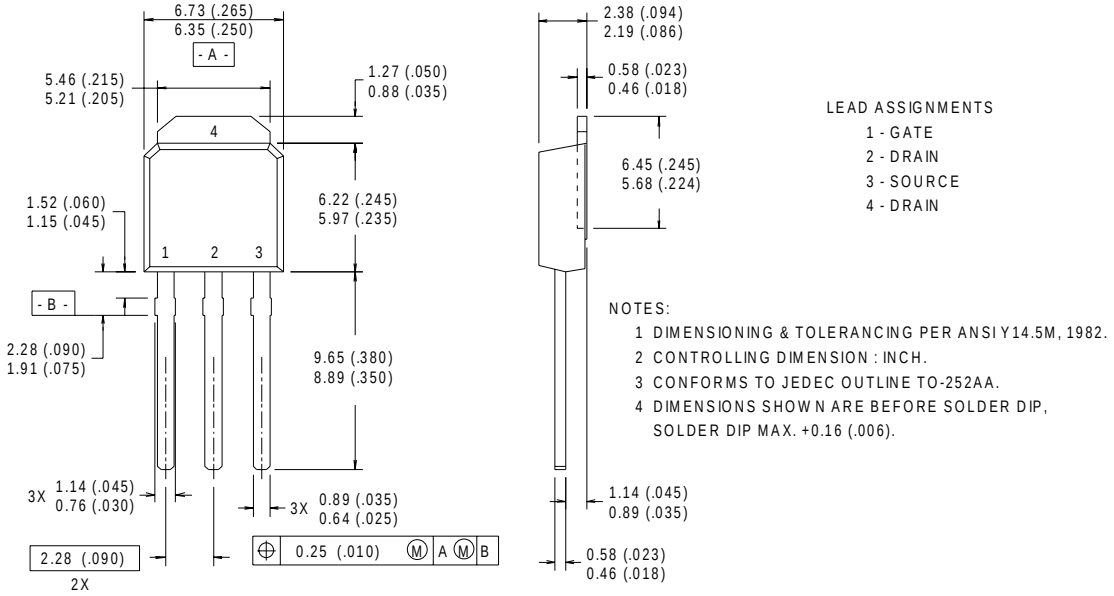
EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



电查网（IC5.CN）— 百万电子工程师爱用电查网

Package Outline

TO-251AA Outline
Dimensions are shown in millimeters (inches)



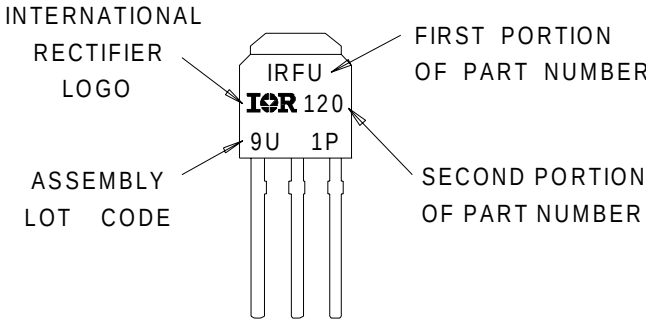
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-251AA (I-PARK)

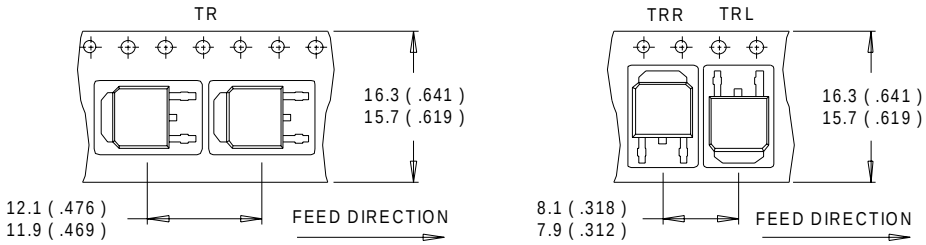
EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P



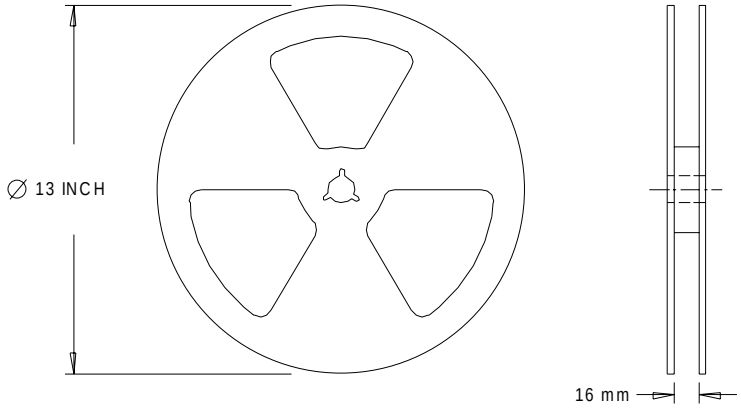
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Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

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IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086
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